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APPLICATION NO. FILING D		ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.			
10/788,518 02/27/2004			02/27/2004	Sumant Ramprasad	030537	6898		
	23696 7590 06/22/2004				EXAM	EXAMINER		
	Qualcomm	-	rated	WAMBACH, MARGARET R				
	Patents Department 5775 Morehouse Drive				ART UNIT	PAPER NUMBER		
	San Diego, CA 92121-1714			2816				
				DATE MAILED: 06/22/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provious of 3 CFR 1.136(a). In no event, however, may a reply be timely filed Extensions of time may be available under the provious of 3 CFR 1.136(a). In no event, however, may a reply be timely filed Extensions of the province of the p		Application No.	Applicant(s)					
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1) Responsive to communication(s) filed on	 THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any 							
2a) ☐ This action is FINAL. 2b) ☐ This action is non-final. 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) ☑ Claim(s)	Status							
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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, 14 and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Alidina et al (hereafter "Alidina".)

As recited in claims 1 and 14, Figure 2 of Alidina et al teaches a shifter circuit capable of shifting a plurality of input data bits (the data word from the source accumulator 24) to the left or right (dependant upon I/r) by a number of bit positions as a function of a binary value of a plurality of shift control bits (shift control bits are stored in auxiliary register 30 which controls the total number of bits shifted by controlling the number of bits shifted at each stage, see column 2, lines 14-21, for instance, Sext is also a shift control bit, see column 2, lines 18-21 and I/r is an additional control bit, see column 2, line 16) comprising a first shifter element or means (18"") configured to perform one of two shifting operations (18"" can shift one bit right or left or not at all as described generically in column 2, lines 31-34 and as also recited in claims 2, 15, please note that if three shifting operations are possible, then it follows that two shifting operations must be possible), a first one of the shift control bits (ar(0)) being used to select the shifting operation of one space right or left or not at all), a second shifter element or means (18"") configured to perform at least one shifting operation (18" can

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shift 2 bits left or right or not at all) on the first output bits to produce a plurality of second output bits (from 18" to 18"), each of said at least one shifting operation being selectable from two shifting operations (again, the two operations being selected from the before mentioned three options), a different one of the control bits (ar(1)) being used to select each of the at least one shifting operation and a third shifter element or means (18") configured to perform one of two shifting operations (18" can shift 4 bits or not depending upon control bit ar(3)) on the second output bits, a second one of the shift control bits (ar(3)) being used to select the shifting operation performed by the third shifter element.

With regard to claim 9, neither the first or second shifter elements of Alidina lose any data bits although the values within the data bits are shifted, thus, in accordance with the commonly accepted meaning of the word "retain", the limitations of claim 9 are met.

With regard to claim 22, a method of shifting a plurality of input data bits (the data word from the source accumulator 24) to the left or right (dependant upon I/r) by a number of bit positions as a function of a binary value of a plurality of shift control bits (shift control bits are stored in auxiliary register 30 which controls the total number of bits shifted by controlling the number of bits shifted at each stage, see column 2, lines 14-21, for instance, Sext is also a shift control bit, see column 2, lines 18-21 and I/r is an additional control bit, see column 2, line 16) comprising performing a shifting operation on the input data bits (18"" is configured to perform one of two shifting operations (18"" can shift one bit right or left or not at all as described generically in column 2, lines 31-

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34 and **as also recited in claim 23**, please note that if three shifting operations are possible, then it follows that two shifting operations must be possible) and using a first one of the shift control bits (ar(0)) to select the shifting operation, performing at least one shifting operation on the first output bits (18" is configured to accept the output from 18" and shift 2 bits left or right or not at all) to produce a plurality of second output bits (from 18" to 18"), a different one of the control bits (ar(1)) being used to select each of the at least one shifting operation and performing a shifting operation on the second output bits (18" is configured to accept the second output bits and shift 4 bits or not) and using a second one of the shift control bits (ar(3)) to select the shifting operation.

Allowable Subject Matter

Claims 3-8, 10-13, 16-21 and 24-32 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Margaret R Wambach whose telephone number is (571)272- 1756. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday 6am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Margaret R Wambach Primary Examiner Art Unit 2816

mrw